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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

First Named Inventor	: Haines et al.	
Appln. No.	: 09/894,821	
Filed	: June 28, 2001	Group Art Unit: 2188
For	: SEQUENTIAL VECTORED BUFFER MANAGEMENT	Examiner: Gary J. Portka
Docket No.	: S01.12-0711/STL 9608	

SUBSTITUTE BRIEF FOR APPELLANT

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20th DAY OF DECEMBER 2005.
A Rego
PATENT ATTORNEY

Sir:

This is an appeal from an Office Action dated April 20, 2004 in which claims 1-2, 9-10 and 20 were finally rejected and claims 3-8 and 11-19 were objected to.

REAL PARTY IN INTEREST

Seagate Technology LLC, a corporation organized under the laws of the state of Delaware, and having offices at 920 Disc Drive, Scotts Valley, California 95066, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment filed with the patent application and recorded on Reel 012663, Frame 0538.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF THE CLAIMS

I. Total number of claims in the application.

	Claims in the application are:	1-20
II. Status of all the claims.		
A.	Claims cancelled:	---
B.	Claims withdrawn but not cancelled:	---
C.	Claims pending:	1-20
D.	Claims objected to but allowable:	3-8 and 11-19
E.	Claims rejected:	1-2, 9-10 and 20.
III. Claims on appeal		
	The claims on appeal are:	1-2, 9-10 and 20.

STATUS OF AMENDMENTS

No amendments were filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

In general, embodiments of the present invention relate to a memory management system having at least one data storage medium and a buffer memory (such as a disc drive, for example).

In traversing a buffer memory, a traversal engine has traditionally functioned such that each access of a subsequent buffer or cache address was treated as a completely new and independent access to the cache. Therefore, even in situations where the traversal engine was to traverse three sequential buffer memory addresses, the traversal engine would release ownership of the buffer and re-arbitrate for access to each subsequent (or "next") buffer address location. This adds significant delay in the command overhead. (Page 3, lines 4-11.)

Embodiments of the present invention address the above-noted problems with the prior art. Independent claim 1 relates to a memory management system 200 (FIGS. 2 and 3) that includes an arbitrated buffer memory 212 having a plurality of memory address locations storing data associated with addresses of a data storage medium 106 (FIG. 1). The system 200 also includes a

traversal component 220 configured to receive a requested traversal, arbitrate ownership of the memory 212 and to traverse sequentially mapped entries in the memory 212, associated with the requested traversal, prior to de-arbitrating itself from ownership of the memory 212. (Page 16, line 24 - page 17, line 6.)

Independent claim 9, which is similar to independent claim 1, is directed to a method of managing a data buffer. The method includes receiving a traversal request to traverse the data buffer (212 of FIGS. 2 and 3) and arbitrating for ownership of the data buffer 212. All sequential entries in the data buffer 212 are traversed, beginning at an entry point in the data buffer 212, corresponding to the traversal request prior to voluntarily relinquishing ownership of the data buffer 212. (Page 18, lines 1-7.)

Independent claim 20, which is similar to independent claims 1 and 9, is written-in means-plus-function form and is directed to a data storage device. The device includes a data storage medium, and means for buffering data written to and read from the data storage medium by utilizing sequentially mapped buffer data, associated with a requested traversal, to decrease time associated with buffering. The structure corresponding to the means element can be found at FIG. 2 (for example) and includes an arbitrated buffer memory 212 and a traversal component 220 configured to receive a requested traversal, arbitrate ownership of the memory 212 and to traverse sequentially mapped entries in the memory 212, associated with the requested traversal, prior to de-arbitrating itself from ownership of the memory 212. (Page 16, line 24 - page 17, line 6.)

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-2, 9 and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Krantz in view of Berning.

Claim 10 (which depends from claim 9) was rejected under 35 U.S.C. §103(a) as being unpatentable over Krantz in view of Berning and further in view of Tamura.

ARGUMENT

I. Description of References Relied on by the Examiner

Krantz et al., U.S. Patent No. 6,530,000 B1, hereinafter "Krantz," relates in general, to a method of providing access to a buffer memory of a hard disk controller. (Col. 1, lines 11-12.) More specifically, Krantz provides a method in which each one of several units or circuits (such as a controller microprocessor, a host interface unit, a disk formatter unit, etc.), within the controller, accesses the buffer memory to store or retrieve information. For example, in one embodiment disclosed in Krantz, the system operates in a cycle during which each unit is offered continuous access duration. The disk formatter, having the most critical access requirements, is offered period access such that the time delay during which it does not have access does not exceed a specified period. (Col. 1, line 63 - col. 2, line 19.)

Berning et al., U.S. Patent No. 6,038,619, hereinafter "Berning," relates to the identification and handling of consecutive read or write requests imposed on a disk drive. (Col. 3, lines 8-9). "Consecutive" read or write requests disclosed in Berning are defined as "pure" or "near" sequential. (Col. 3, line 11). To determine that, logical block addresses (LBAs), which are an addressing scheme used to access locations on the disk 11 in Berning, are compared between current and immediate predecessor requests. (Col. 3, lines 30-31).

Tamura, U.S. Patent No. 6,389,508, relates to an information storing apparatus such as a magnetic disk drive or the

like for writing data transferred by a write command from a host onto a medium. (Col. 1, lines 5-8).

II. Claim Rejections

In section 3 of the final Office Action, claims 1-2 and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over Krantz in view of Berning. Further, claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Krantz in view of Berning and further in view of Tamura.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. In re Vaeck, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. §2143.

Under these criteria, the final Office Action fails to establish a *prima facie* case of obviousness of claims 1-2 and 9-10 based on the cited prior art.

Argument for claims 1 and 2

Claim 1 includes an arbitrated buffer memory and a traversal component configured to traverse sequentially mapped entries in the memory. As correctly pointed out in the final Office Action, Krantz does not disclose a traversal component configured to traverse sequentially mapped entries in an arbitrated buffer memory. In fact, Krantz makes no suggestion of that feature. As a result, the final Office Action relies on Berning. (Citing Abstract, col. 2 lines 64-67, and col. 3, lines 8-24 and 25-40.)

The final Office Action states, with respect to Berning, that the "teaching of allowing the traversal of sequential entries unabated as applied to Krantz is clearly equal

to the recited traversal of entries prior to de-arbitrating." This statement is incorrect.

Berning discloses a data buffer 7 that is distinct from the disk 11 (see FIG. 1). "Consecutive" read and write requests disclosed in that reference are defined as "pure" or "near" sequential (col. 3, line 11). To determine that, logical block addresses (LBAs) are compared between current and immediate predecessor requests. One skilled in the art understands that LBAs is an addressing scheme used to access the disk 11 (see col. 2, lines 55-61). In fact, each discussion of sequential logical addresses is associated with features of the disk, such as "(cylinder, track, and head)" in col. 2, lines 55-61, and "a cyclic, concentric, multitracked disk or a cyclic, spiraltracked disk," in col. 3, lines 28-37. Thus, Berning deals with consecutive requests to the disk 11, not to data buffer 7. In addition, Berning does not teach or suggest traversing sequentially mapped entries in a buffer memory prior to de-arbitrating ownership of the buffer memory, as recited in claim 1.

The buffer memory is a different element than the recited data storage medium in claim 1. Since neither reference teaches nor suggests a traversal component configured to traverse sequentially mapped entries in an arbitrated buffer memory, the Examiner has failed to support a *prima facie* conclusion of obviousness (by not satisfying the third criterion for a *prima facie* conclusion of obviousness set forth in Vaeck) with regard to claim 1. Therefore, claim 1 is allowable. Claim 2 is also allowable due to its dependence on allowable claim 1.

In response to the Appellants' arguments to a previous Office Action, the final Office Action states "Berning describes requests for sequential entries in the device, and the description that this data is 'streamed' through the buffer necessarily includes that sequential data is consecutively accessed in the buffer." The phrase "necessarily includes that sequential data is

consecutively accessed in the buffer" is entirely conclusory and, in reality, is nothing more but an inherency argument.

Section 2112 of the Manual of Patent Examination and Procedure (MPEP) states that:

> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990).

Appellants respectfully submit that, without providing the necessary support required in accordance with the above MPEP section, the Examiner has not met the burden required to support the rejection of claim 1 under 35 U.S.C. §103(a).

The final Office Action cites to no reference to support the conclusion "necessarily includes that sequential data is consecutively accessed in the buffer." No evidence of record exists that shows one skilled in the art would recognize such. No logical reasoning is provided, based on objective evidence, that supports this conclusion. The final Office Action simply provides nothing to show that traversing "sequentially mapped entries in the memory, associated with the requested traversal, prior to de-arbitrating itself from ownership of the memory" is inherent in Berning or known to one skilled in the art.

As mentioned above, traditional traversal engines have functioned such that even in situations were the traversal engine was to traverse sequential buffer memory addresses, the traversal engine would release ownership of the buffer and re-arbitrate for access to each subsequent (or "next") buffer address location. To overcome these problems, claim 1 includes a traversal component configured to receive a requested traversal, arbitrate ownership of the memory and to traverse sequentially mapped entries in the memory, associated with the requested traversal, prior to de-

arbitrating itself from ownership of the memory. This is clearly not inherent in the teachings of Berning.

Thus, the Examiner's apparent conclusion of inherency is not correct and not supported by the reference. However, even if the Examiner's conclusion of inherency were correct, it would have no legal support on which to base an obviousness type rejection. "That which may be inherent is not necessarily known. Obviousness cannot be predicated on what is unknown." In re Spormann, 363 F.2d 444, 448, 150 USPQ 449, 452 (CCPA 1966) (emphasis added). For the above reasons, a *prima facie* case of obviousness for claim 1 has not been made. Thus, claim 1 is allowable.

Argument for claim 9

Claim 9 features traversing all sequential entries in the data buffer. Krantz teaches or suggests nothing about accessing entries in the data buffer. Similarly, Berning teaches or suggests nothing about traversing all sequential entries in the data buffer. Therefore, claim 9 is not obvious and is allowable.

Argument for claim 10

As mentioned above, claim 10 (which depends from claim 9) was rejected under 35 U.S.C. §103(a) as being unpatentable over Krantz in view of Berning and further in view of Tamura. As explained above, claim 9 is not obvious in view of Krantz and Berning. Tamura does not overcome the deficiencies of those references. As such, claim 10 is also not obvious over those references due to its dependence on allowable claim 9.

Argument for claim 20

Claim 20 was rejected under 35 U.S.C. §103(a) as being unpatentable over Krantz in view of Berning.

Claim 20 is written-in "means-plus-function" form and includes "means for buffering data written to and read from the data storage medium by utilizing sequentially mapped buffer data, associated with a requested traversal, to decrease time associated

with buffering." In examining a means-plus-function claim, the Supplemental Examination Guidelines for Determining the Applicability of 35 U.S.C. § 112, Paragraph 6, which were set forth in the Federal Register on June 21, 2000 (Vol. 65, No. 120) apply. (See also In re Donaldson Co., 29 U.S.P.Q.2d 1845 (Fed. Cir. 1994) and IMS Technology, Inc. v. Haas Automation, Inc., 54 U.S.P.Q.2d 1129 (Fed. Cir. 2000)). Section II, paragraph 2 of the Guidelines, states "If a claim limitation invokes 35 U.S.C. § 112, para 6, it must be interpreted to cover the corresponding structure, material or acts in the specification and 'equivalents thereof.'"

In the present case, independent claim 20 recites means for buffering data written to and read from the data storage medium by utilizing sequentially mapped buffer data, associated with a requested traversal, to decrease time associated with buffering. Thus, according to the Guidelines, the structure (i.e., means for buffering data written to and read from the data storage medium by utilizing sequentially mapped buffer data, associated with a requested traversal, to decrease time associated with buffering) shall be construed as disclosed in Appellants' Specification. The corresponding structure can be found at FIG. 2 (for example) and includes an arbitrated buffer memory 212 and a traversal component 220 configured to receive a requested traversal, arbitrate ownership of the memory 212 and to traverse sequentially mapped entries in the memory 212, associated with the requested traversal, prior to de-arbitrating itself from ownership of the memory 212.

As mentioned above, Krantz teaches or suggests nothing about accessing entries in the data buffer. Further, as noted above, Berning teaches or suggested nothing about traversing all sequential entries in the data buffer. Therefore, a properly interpreted means-plus-function claim 16 is non-obvious over the cited prior art.

CONCLUSION

For the reasons discussed above, Appellants respectfully submit that claims 1-2, 9-10 and 20 are neither taught nor suggested by the references cited by the Examiner. Thus, Appellants respectfully request that the Board reverse the Examiner and find all pending claims allowable.

Respectfully submitted,

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Claims Appendix

1. A memory management system having at least one data storage medium, the memory management system comprising:

an arbitrated buffer memory having a plurality of memory address locations storing data associated with addresses of the data storage medium; and

a traversal component configured to receive a requested traversal, arbitrate ownership of the memory and to traverse sequentially mapped entries in the memory, associated with the requested traversal, prior to de-arbitrating itself from ownership of the memory.

2. The memory management system of claim 1 wherein the traversal component comprises:

a memory accessing component sequentially accessing entries in the memory based on the requested traversal and storing the entries in an accessing memory.

3.(Pending but not on appeal) The memory management system of claim 2 wherein the traversal component comprises:

a traversal engine configured to access the entries in the accessing memory and determine whether the entries in the accessing memory correspond to memory entries corresponding to the requested traversal.

4.(Pending but not on appeal) The memory management system of claim 3 wherein the memory comprises a linked list of memory locations.

5.(Pending but not on appeal) The memory management system of claim 4 wherein the requested traversal includes a memory

starting address and a number of hops to take through the linked list beginning at the memory starting address.

6.(Pending but not on appeal) The memory management system of claim 5 wherein the traversal engine is configured to determine whether the entries in the accessing memory correspond to memory entries corresponding to the requested traversal by determining whether the entries in the accessing memory correspond to memory locations in the linked list identified by the requested traversal.

7.(Pending but not on appeal) The memory management system of claim 6 wherein the memory accessing component and the traversal engine are configured to operate substantially in parallel.

8.(Pending but not on appeal) The memory management system of claim 7 wherein the traversal component is configured to voluntarily relinquish ownership of the memory after traversing sequentially mapped entries in the memory and to re-arbitrate for ownership of the memory and continuing traversal of the memory until the requested traversal is complete.

9. A method of managing a data buffer, the method comprising:
   (a) receiving a traversal request to traverse the data buffer;
   (b) arbitrating for ownership of the data buffer; and
   (c) traversing all sequential entries in the data buffer, beginning at an entry point in the data buffer, corresponding to the traversal request prior to voluntarily relinquishing ownership of the data buffer.

10. The method of claim 9 wherein receiving operation (a) comprises:

(a)(1) receiving a data buffer starting address; and

(a)(2) receiving a number of memory locations in the data buffer which must be made to complete the traversal request.

11.(Pending but not on appeal) The method of claim 10 wherein the data buffer comprises a linked list and wherein the traversing operation (c) comprises:

(c)(1) reading adjacent entries in the data buffer into a register; and

(c)(2) determining whether the entries in the register correspond to the traversal request.

12.(Pending but not on appeal) The method of claim 11 wherein the traversing operation (c) further comprises:

performing the reading operation (c)(1) and the determining operation (c)(2) substantially in parallel.

13.(Pending but not on appeal) The method of claim 12 wherein the traversing operation (c) further comprises:

(c)(3) reducing the number of memory locations from the receiving operation (a)(2) by one each time the determining operation (c)(2) determines that an entry in the register corresponds to the traversal request.

14.(Pending but not on appeal) The method of claim 13 and further comprising:

(d) voluntarily relinquishing ownership of the data buffer after all sequential entries in the data buffer, corresponding to the traversal request, are read into the register.

15.(Pending but not on appeal) The method of claim 13 and

further comprising:

(e) stopping the reading operation (c)(1) when it is determined in determining operation (c)(2) that an entry in the register does not correspond to the traversal request; and

(f) voluntarily relinquishing ownership of the data buffer.

16.(Pending but not on appeal) The method of claim 15 and further comprising:

(g) after ownership of the data buffer has been relinquished, determining whether the number of memory locations from the receiving operation (a)(2) has been reduced to zero.

17.(Pending but not on appeal) The method of claim 16 and further comprising:

(h) if in step (g) it is determined that the number of memory locations from the receiving operation (a)(2) has not been reduced to zero, re-arbitrating for ownership of the data buffer.

18.(Pending but not on appeal) The method of claim 17 and further comprising:

(i) continuing the traversing operation (c) until the number of memory locations to complete the traversal request is reduced to zero.

19.(Pending but not on appeal) The method of claim 18 wherein the continuing operation (i) comprises:

(i)(1) beginning traversing the data buffer at an entry point at a next data buffer location in the linked list corresponding to the traversal request.

20. A data storage device, comprising:

a data storage medium; and

means for buffering data written to and read from the data storage medium by utilizing sequentially mapped buffer data, associated with a requested traversal, to decrease time associated with buffering.

Evidence Appendix

None.

Related Proceedings Appendix

There are no known related appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.